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# R1LV0408D Series

4M SRAM (512-kword × 8-bit)

REJ03C0310-0100

Rev.1.00

May.24.2007

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## Description

The R1LV0408D is a 4-Mbit static RAM organized 512-kword × 8-bit, fabricated by Renesas's high-performance 0.15 $\mu$ m CMOS and TFT technologies. R1LV0408D Series has realized higher density, higher performance and low power consumption. The R1LV0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin STSOP.

## Features

- Single 3 V supply: 2.7 V to 3.6 V
- Access time: 55/70 ns (max)
- Power dissipation:
  - Standby: 3  $\mu$ W (typ)
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Directly TTL compatible.
  - All inputs and outputs
- Battery backup operation.

## R1LV0408D Series

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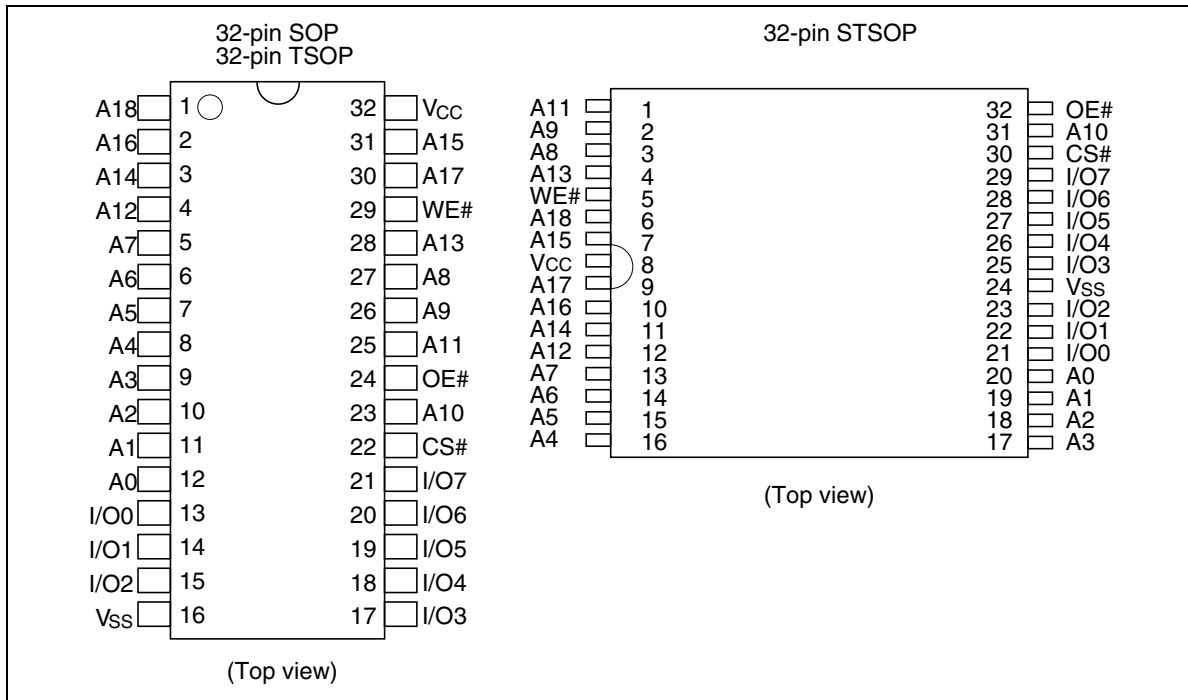
### Ordering Information

Type No.	Access time	Package
R1LV0408DSP-5S%	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LV0408DSP-7L%	70 ns	
R1LV0408DSB-5S%	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LV0408DSB-7L%	70 ns	
R1LV0408DSA-5S%	55 ns	8mm × 13.4mm STSOP (32P3K-B)
R1LV0408DSA-7L%	70 ns	

?: Temperature version; see table below.

?	Temperature Range
R	0 to +70°C
I	-40 to +85°C

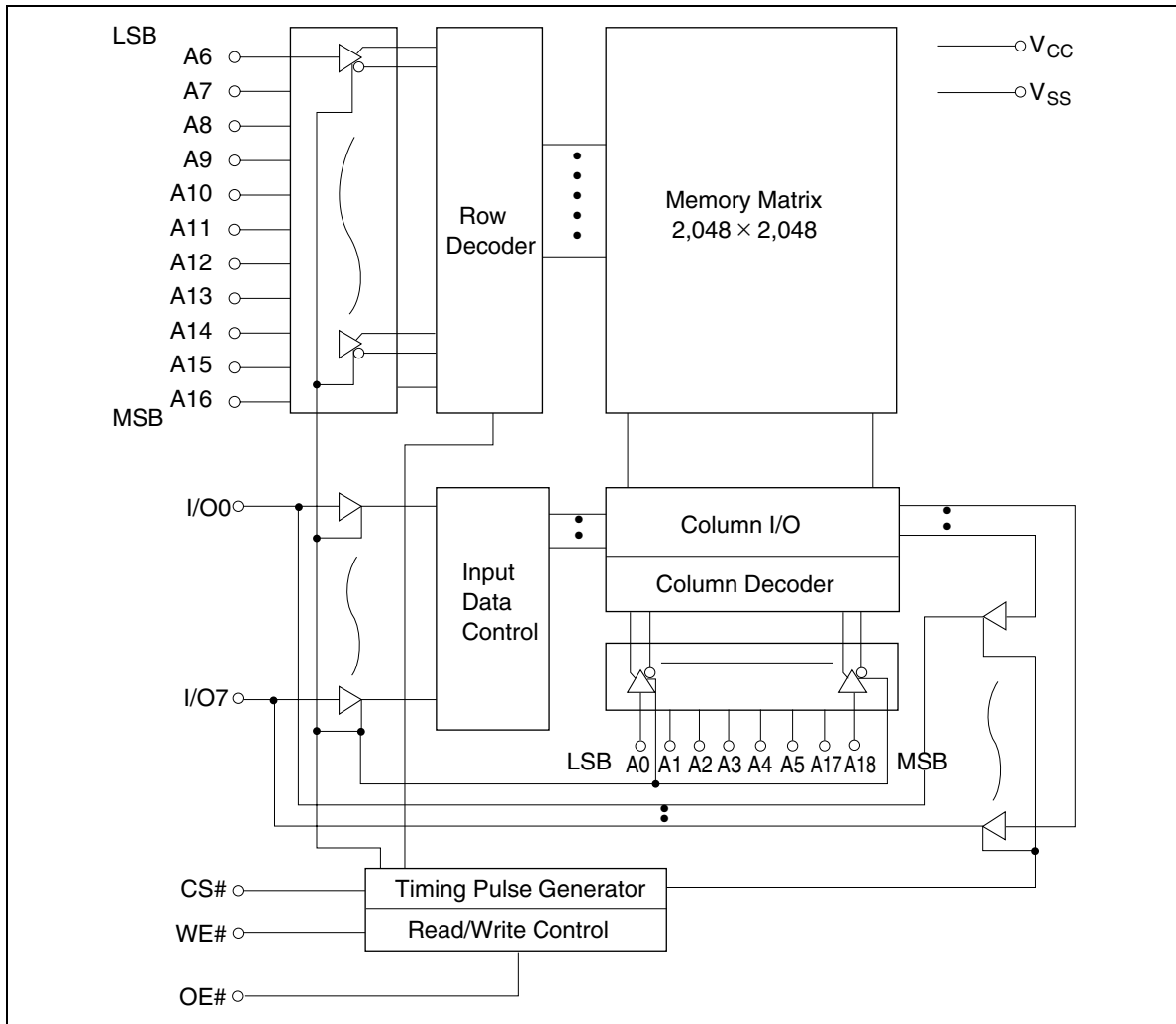
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# ( $\overline{CS}$ )	Chip select
OE# ( $\overline{OE}$ )	Output enable
WE# ( $\overline{WE}$ )	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

Block Diagram



## Operation Table

WE#	CS#	OE#	Mode	V <sub>CC</sub> current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I <sub>SB</sub> , I <sub>SB1</sub>	High-Z	—
H	L	H	Output disable	I <sub>CC</sub>	High-Z	—
H	L	L	Read	I <sub>CC</sub>	Dout	Read cycle
L	L	H	Write	I <sub>CC</sub>	Din	Write cycle (1)
L	L	L	Write	I <sub>CC</sub>	Din	Write cycle (2)

Note: H: V<sub>IH</sub>, L: V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Terminal voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5* <sup>2</sup>	V
Power dissipation	P <sub>T</sub>	0.7	W
Operating temperature	Topr	R ver.	0 to +70
		I ver.	-40 to +85
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	R ver.	0 to +70
		I ver.	-40 to +85

Notes: 1. V<sub>T</sub> min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +4.6 V.

## DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3* <sup>1</sup>	—	0.6	V
Ambient temperature range	R ver.	Ta	0	+70	°C
	I ver.		-40	+85	

Note: 1. V<sub>IL</sub> min: -3.0 V for pulse half-width ≤ 30 ns.

## DC Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input leakage current		$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$	
Output leakage current		$ I_{LO} $	—	—	1	$\mu\text{A}$	CS# = $V_{IH}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ or $V_{IO} = V_{SS}$ to $V_{CC}$	
Operating current		$I_{CC}$	—	—	10	mA	CS# = $V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA	
Average operating current		$I_{CC1}$	—	—	25	mA	Min. cycle, duty = 100%, CS# = $V_{IL}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA	
		$I_{CC2}$	—	—	5	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{IO} = 0$ mA, CS# $\leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V	
Standby current		$I_{SB}$	—	0.1*1	0.3	mA	CS# = $V_{IH}$	
Standby current	-5S%	to +85°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	Average values $V_{in} \geq 0$ V, CS# $\geq V_{CC} - 0.2$ V
		to +70°C	$I_{SB1}$	—	—	8	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	3	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	1*1	2.5	$\mu\text{A}$	
	-7L%	to +85°C	$I_{SB1}$	—	—	20	$\mu\text{A}$	
		to +70°C	$I_{SB1}$	—	—	16	$\mu\text{A}$	
		to +40°C	$I_{SB1}$	—	—	10	$\mu\text{A}$	
		to +25°C	$I_{SB1}$	—	1*1	10	$\mu\text{A}$	
Output low voltage		$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA	
		$V_{OL2}$	—	—	0.2	V	$I_{OL} = 100$ $\mu\text{A}$	
Output high voltage		$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0$ mA	
		$V_{OH2}$	$V_{CC} - 0.2$	—	—	—	V	$I_{OH} = -0.1$ mA

Note: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0$  MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{IO}$	—	—	10	pF	$V_{IO} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$  /  $-40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (50 pF) (R1LV0408D-5S%)  
1 TTL Gate +  $C_L$  (100 pF) (R1LV0408D-7L%)  
(Including scope and jig)

Note: Temperature range depends on R/I-version. Please see table on page 2.

### Read Cycle

Parameter	Symbol	R1LV0408D				Unit	Notes
		-5S%		-7L%			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	55	—	70	—	ns	
Address access time	$t_{AA}$	—	55	—	70	ns	
Chip select access time	$t_{CO}$	—	55	—	70	ns	
Output enable to output valid	$t_{OE}$	—	30	—	35	ns	
Chip select to output in low-Z	$t_{LZ}$	10	—	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2
Chip deselect to output in high-Z	$t_{HZ}$	0	20	0	25	ns	1, 2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2
Output hold from address change	$t_{OH}$	10	—	10	—	ns	

**Write Cycle**

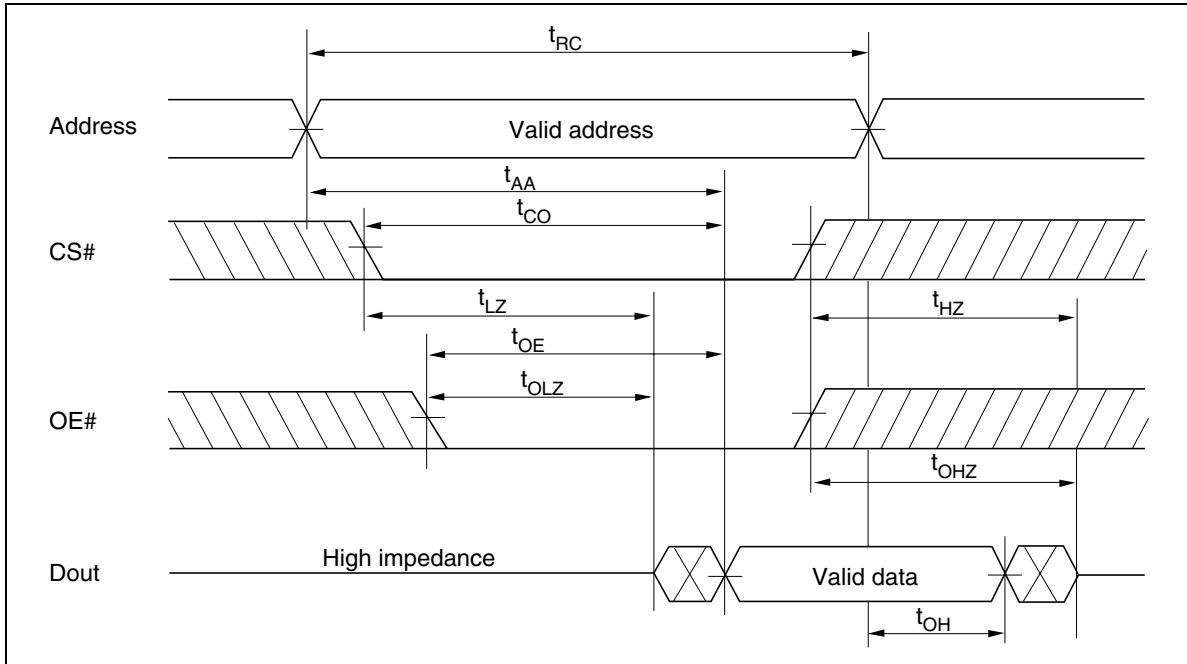
Parameter	Symbol	R1LV0408D				Unit	Notes
		-5S%		-7L%			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	55	—	70	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	60	—	ns	4
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Address valid to end of write	$t_{AW}$	50	—	60	—	ns	
Write pulse width	$t_{WP}$	40	—	50	—	ns	3, 12
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	25	—	30	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1, 2, 7

- Notes:
- $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - A write occurs during the overlap ( $t_{WP}$ ) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from CS# going low to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earlier of WE# or CS# going high to the end of write cycle.
  - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
  - If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
  - Dout is the same phase of the write data of this write cycle.
  - Dout is the read data of next address.
  - If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  - In the write cycle with OE# low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

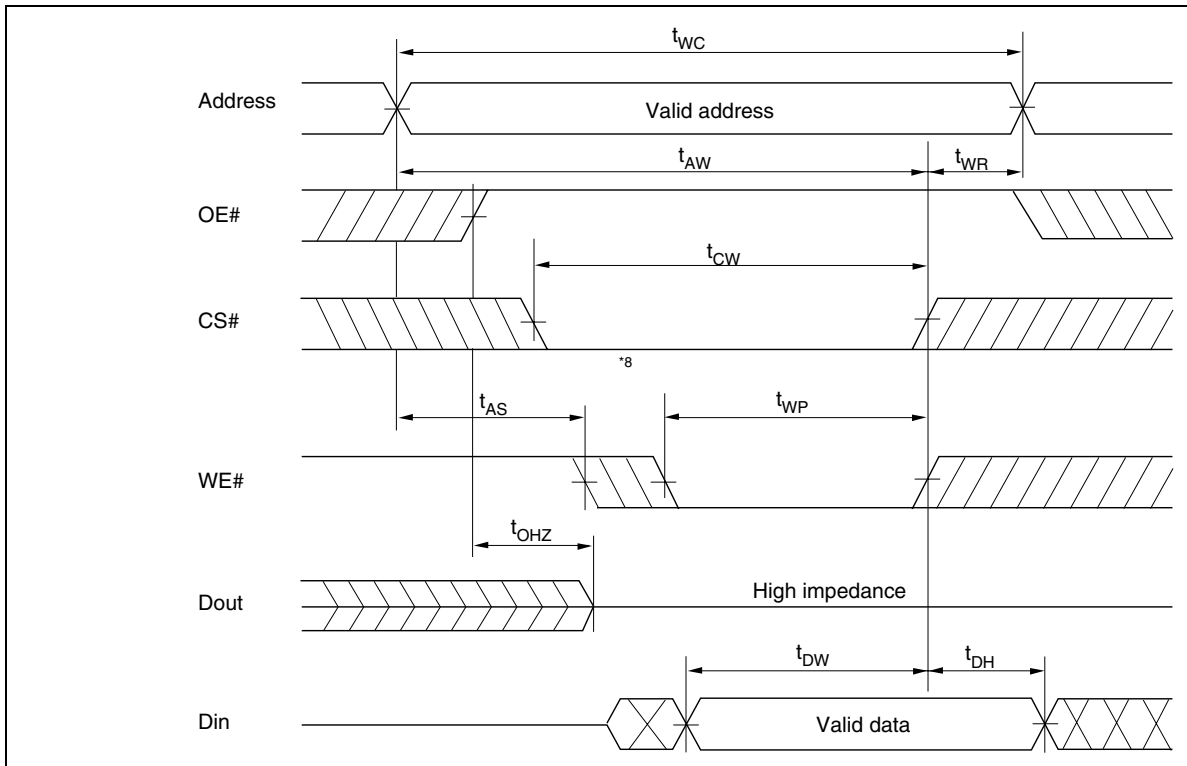


## Timing Waveform

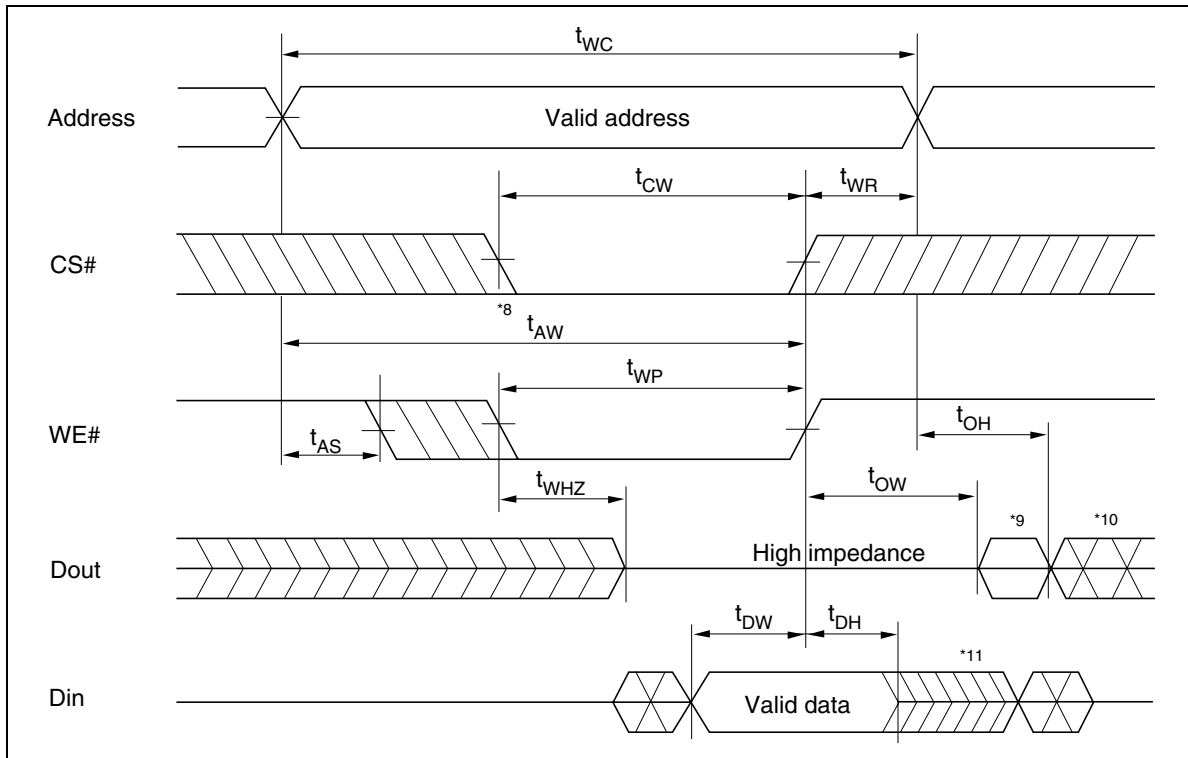
### Read Timing Waveform (WE# = V<sub>ih</sub>)



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



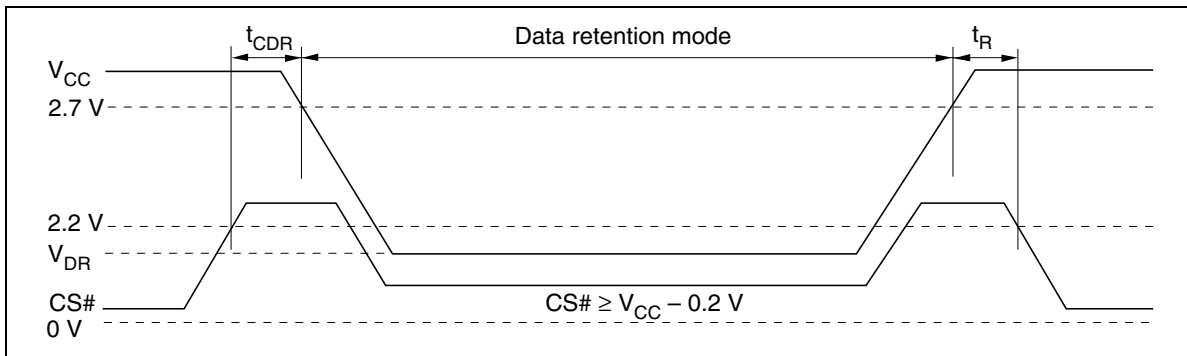
### Low V<sub>CC</sub> Data Retention Characteristics

(T<sub>a</sub> = 0 to +70°C / -40 to +85°C)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
V <sub>CC</sub> for data retention		V <sub>DR</sub>	2	—	—	V	CS# ≥ V <sub>CC</sub> - 0.2 V, Vin ≥ 0 V	
Data retention current	-5S%	to +85°C	I <sub>CCDR</sub>	—	—	10	μA	V <sub>CC</sub> = 3.0 V, Vin ≥ 0 V CS# ≥ V <sub>CC</sub> - 0.2 V Average values
		to +70°C	I <sub>CCDR</sub>	—	—	8	μA	
		to +40°C	I <sub>CCDR</sub>	—	—	3	μA	
		to +25°C	I <sub>CCDR</sub>	—	1* <sup>1</sup>	2.5	μA	
	-7L%	to +85°C	I <sub>CCDR</sub>	—	—	20	μA	
		to +70°C	I <sub>CCDR</sub>	—	—	16	μA	
		to +40°C	I <sub>CCDR</sub>	—	—	10	μA	
		to +25°C	I <sub>CCDR</sub>	—	1* <sup>1</sup>	10	μA	
Chip deselect to data retention time		t <sub>CDR</sub>	0	—	—	ns	See retention waveform	
Operation recovery time		t <sub>R</sub>	5	—	—	ms		

Note: 1. Typical values are at V<sub>CC</sub> = 3.0 V, T<sub>a</sub> = +25°C and specified loading, and not guaranteed.

### Low V<sub>CC</sub> Data Retention Timing Waveform (CS# Controlled)



**Revision History****R1LV0408D Series Data Sheet**

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Dec. 25, 2006	—	Initial issue
1.00	May. 24, 2007	6	DC Characteristics $I_{SB1}$ (-5S%) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A
		12	Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ (-5S%) (to +25°C) max: 3 $\mu$ A to 2.5 $\mu$ A Deletion of note 2

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